

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) Mirror suppression circuit comprising

a first quadrature signal path coupled between quadrature signal input and output terminals and including

an error correction circuit for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components,

characterized by wherein

~~a quadrature output of said-the~~ error correction circuit ~~being-is~~ coupled through a first filter circuit for a selection of ~~said-the~~ quadrature signal to a first quadrature input of an error detection circuit,

~~said-the~~ first quadrature signal path ~~being-is~~ coupled prior to ~~said-the~~ first filter circuit through a second quadrature signal path to a second quadrature input of ~~said-the~~ error detection circuit,

~~said-the~~ error detection circuit ~~detecting-detects~~ amplitude and phase errors and ~~providing-provides~~ amplitude and phase control signals to amplitude and phase control inputs of ~~said-the~~ error correction circuit for a negative feed back of ~~said-the~~ amplitude and phase errors to ~~said-the~~ error correction circuit,

~~said-the~~ amplitude control signal ~~varying-varies~~ with at least one of products $I_w * I_{ref}$ and $Q_w * Q_{ref}$, and

~~said-the~~ phase control signal ~~varying-varies~~ with at least one of products $I_w * Q_{ref}$ and $Q_w * I_{ref}$,

I_w and Q_w , respectively I_{ref} and Q_{ref} , representing the in-phase and phase quadrature signal components of ~~said-the~~ quadrature signal at the first quadrature input of the error detection circuit, ~~respectively-and~~ I_{ref} and Q_{ref} representing the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier frequency of ~~said-the~~ quadrature signal at the second quadrature input of the error detection circuit.

2. (Currently amended) Mirror suppression circuit according to claim 1, wherein characterized by

said the amplitude control signal varying varies with $I_w * I_{ref} + Q_w * Q_{ref}$, and said the phase control signal varying varies with $I_w * Q_{ref} - Q_w * I_{ref}$.

3. (Currently amended) Mirror suppression circuit according to claim 1, wherein or 2, characterized by

the second quadrature signal path including includes

an inverter means providing that provides signal inversion in obtaining said the quadrature reference signal.

4. (Currently amended) Mirror suppression circuit according to claim 1, wherein one of claims 1 to 3, characterized by

said the second quadrature signal path being is coupled to the first quadrature signal path subsequent to the error correction circuit.

5. (Currently amended) Mirror suppression circuit according to claim 1, wherein one of claims 1 to 4, characterized by

said the second quadrature signal path including includes a second filter circuit for a selection of said the quadrature reference signal.

6. (Currently amended) Mirror suppression circuit according to claim 3, wherein one of claims 3 to 5, characterized by

said the second quadrature signal path comprising said signal includes the inverter coupled between the first quadrature signal path and said the second filter circuit,

said the second filter circuit being substantially identical to said the first filter circuit.

7. (Currently amended) Receiver providing quadrature signal processing comprising
 an RF input stage subsequently followed by a mixer stage for a conversion of an RF
 signal into an IF signal ~~and~~,
 an IF stage for a selective amplification of ~~said the~~ IF signal, ~~and~~
characterized by
a mirror suppression circuit according to one of claims 1 to 5 comprising
a first quadrature signal path coupled between quadrature signal input and output
terminals and including
an error correction circuit for correction of amplitude and phase errors in a
carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal
components,
wherein
a quadrature output of the error correction circuit is coupled through a first filter
circuit for a selection of the quadrature signal to a first quadrature input of an error detection
circuit,
the first quadrature signal path is coupled prior to the first filter circuit through a
second quadrature signal path to a second quadrature input of the error detection circuit,
the error detection circuit detects amplitude and phase errors and provides amplitude
and phase control signals to amplitude and phase control inputs of the error correction circuit
for a negative feed back of the amplitude and phase errors to the error correction circuit,
the amplitude control signal varies with at least one of products $I_w * I_{ref}$ and $Q_w * Q_{ref}$,
the phase control signal varies with at least one of products $I_w * Q_{ref}$ and $Q_w * I_{ref}$,
 I_w and Q_w representing the in-phase and phase quadrature signal components of
the quadrature signal at the first quadrature input of the error detection circuit, and I_{ref} and Q_{ref}
representing the in-phase and phase quadrature signal components of a quadrature reference
signal occurring at the negative carrier frequency of the quadrature signal at the second
quadrature input of the error detection circuit,
having its the quadrature signal input of the mirror suppression circuit is coupled to a
quadrature output of the mixer stage, and
said the first filter circuit being is part of said the IF stage and having has a resonance
frequency at the carrier frequency of said the IF signal.

8. (Currently amended) Receiver according to claim 7, wherein comprising
a mirror suppression circuit according to claim 5,
characterized by
the second quadrature signal path includes a second filter circuit for a selection of the
quadrature reference signal, and
the second filter circuit selecting selects the quadrature reference signal occurring
at the negative carrier frequency of said the quadrature IF signal.

9. (Currently amended) Receiver according to claim 8 comprising
a mirror suppression circuit according to claim 3,
characterized by wherein
the second quadrature signal path includes
an inverter that provides signal inversion in obtaining the quadrature reference
signal, and
said the second quadrature signal path comprising comprises
said signal the inverter coupled between the first quadrature signal path and
said the second filter circuit,
said the second filter circuit being identical to said the IF filter circuit.

10. (Currently amended) Receiver according to claim 9, wherein characterized by
both first and second filter circuits comprising comprise resonance amplifier type
polyphase filters.

11. (Currently amended) Receiver according to claim 7, wherein one of claims 1 to 10,
characterized in that
said the error correction circuit includes
an amplitude correction circuit comprising
a first multiplier included in at least one of the pair of in-phase and
quadrature paths of the first quadrature signal path for an amplitude variation of the signal at
said the input with said the amplitude error.

12. (Currently amended) Receiver according to claim 11, wherein characterized by
said-the amplitude correction circuit comprising comprises
a differential stage following said-the detection circuit converting said-that
converts the amplitude control signal into a differential pair of first and second amplitude
control signals and supplying supplies the same differential pair to said-the first and a second
multiplier, respectively,

said-the first and second multipliers being are included in said-the in-phase and
quadrature paths of the first quadrature signal path.

13. (Currently amended) Receiver according to claim 7, wherein one of claims 1 to 10,
characterized in that

said-the error correction circuit includes a phase correction circuit comprising
a third multiplier having
a signal input coupled to one of said-the in-phase and quadrature paths
of the first quadrature signal path and
a signal output coupled to a first adder device, which is included in the
other of said-the in-phase and quadrature paths for supplying thereto a part of the signal
occurring at said-the one path to said-the other path varying with said-the phase control signal.

14. (Currently amended) Receiver according to claim 13, wherein characterized by
said-the phase correction circuit comprising comprises

a differential stage following said-the detection circuit converting said-that
converts the phase error into a differential pair of first and second phase error signals and
supplying the same supplies the differential pair to modulation signal inputs of said-the third
and a fourth multiplier, respectively, and

said-the third and fourth multipliers having include:

inputs coupled to the phase quadrature and in-phase paths of the first
quadrature signal path, and having

outputs coupled to said-the first and a second adder device, which are included
in said-the in-phase and phase quadrature paths, respectively.

15. (New) Mirror suppression circuit according to claim 2, wherein
the second quadrature signal path includes
an inverter that provides signal inversion in obtaining the quadrature reference
signal.

16. (New) Mirror suppression circuit according to claim 15, wherein
the second quadrature signal path is coupled to the first quadrature signal path
subsequent to the error correction circuit.

17. (New) Mirror suppression circuit according to claim 16, wherein
the second quadrature signal path includes a second filter circuit for a selection of the
quadrature reference signal.

18. (New) Mirror suppression circuit according to claim 17, wherein
the second quadrature signal path includes the inverter coupled between the first
quadrature signal path and the second filter circuit,
the second filter circuit being substantially identical to the first filter circuit.

19. (New) Mirror suppression circuit according to claim 2, wherein
the second quadrature signal path is coupled to the first quadrature signal path
subsequent to the error correction circuit.

20. (New) Mirror suppression circuit according to claim 3, wherein
the second quadrature signal path is coupled to the first quadrature signal path
subsequent to the error correction circuit.